AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 32, 46, 49 and 64 as shown below. The following is a complete list of all claims in this application.

1. (Previously Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer pattern covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming an ohmic contact layer pattern on the semiconductor pattern;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on the ohmic contact layer;

forming color filters, said color filters covering the data wire and having a first contact hole exposing the drain electrode; and

forming a pixel electrode connected to the drain electrode through the first contact hole,

wherein the source electrode and the drain electrode are separated by a photolithography process using a photoresist pattern, and the photoresist pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness larger than the first portion, and a third portion having a third thickness smaller than the first thickness.

2. (Previously Amended) The method of claim 1, wherein the photoresist pattern is formed by a mask that has a first, a second, and a third part, a transmittance of the third part is higher than the first and the second parts, a transmittance of the first part is higher than the second part, and

wherein the photoresist pattern is formed of positive photoresist, and the mask is aligned such that the first, the second, and the third parts respectively face the first, the second, and the third portions of the photoresist pattern in an exposing step.

3. (Original) The method of claim 2, wherein the first part of the mask includes a partially transparent layer.

4. (Original) The method of claim 2, wherein the first part of the mask includes a pattern smaller than the resolution of the exposure used in the exposing step.

5. (Original) The method of claim 1, wherein the first portion is formed by reflow.

6. (Original) The method of claim 1, wherein the thickness of the first portion is less than a half of the thickness of the second portion.

7. (Original) The method of claim 6, wherein the thickness of the second portion is 1μ to 2μ.

8. (Original) The method of claim 7, wherein the thickness of the first portion is less than 4,000 Å.

9. (Original) The method of claim 1, wherein the data wire, the ohmic contact layer pattern, the semiconductor pattern, and the gate insulating layer pattern are formed in the same photolithography process.

10. (Previously Amended) The method of claim 9, wherein steps of forming the gate insulating layer pattern, the semiconductor pattern, the ohmic contact layer pattern, and the data wire comprises:

depositing a gate insulating layer, a semiconductor layer, an ohmic contact layer, and a conductor layer;

coating a photoresist layer on the conductor layer;

exposing the photoresist layer through a mask;

forming the photoresist pattern such that the second portion lies on the data wire by developing the photoresist layer;

forming the data wire, the ohmic contact layer pattern, the semiconductor pattern, and the gate insulating layer pattern that are respectively formed of the conductor layer, the ohmic contact layer, the semiconductor layer, and the gate insulating layer by removing a portion of the conductor layer under the third portion, the semiconductor layer, the ohmic contact layer, and the underlying gate insulating layer, and by removing the first portion, the conductor layer, and the ohmic contact layer under the first portion, and by removing a partial thickness of the second portion; and

removing the photoresist pattern.

11. (Original) The method of claim 10, wherein the step of forming the data wire, the ohmic contact layer pattern, the semiconductor pattern, and the gate insulating layer pattern comprises:

removing the portion of the conductor layer under the third portion by dry etching or wet etching to expose the ohmic contact layer;

dry etching the ohmic contact layer under the third portion, the semiconductor layer, and the underlying gate insulating layer, and the first portion to complete a semiconductor pattern and a gate insulating layer pattern, along with exposing the substrate or the gate insulating layer under the third portion and the conductor layer under the first portion; and

removing the conductor layer under the first portion and the underlying ohmic contact layer to complete a data wire and a ohmic contact layer pattern.

12. (Previously Amended) The method of claim 1, wherein the gate wire further includes a gate pad that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and the color filters have a second contact hole and a third contact hole respectively exposing the gate pad and the data pad,

further comprising a step of forming a redundant gate pad and a redundant data pad that are formed of the same layer as the pixel electrode and are respectively connected to the gate pad and the data pad through the second contact hole and the third contact hole.

29. (Previously Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode, a drain electrode and a data line connected to the source electrode on the semiconductor pattern, wherein the gate insulating layer, the semiconductor pattern and the data wire are patterned in a single photolithography step;

forming color filters formed of a photosensitive material and covering the data wire;

forming a passivation layer covering the color filers;

forming a first contact hole extending to the drain electrode via the passivation layer and the color filters; and

forming a pixel electrode connected to the drain electrode through the first contact hole.

30. (Currently Amended) The method of claim 29, wherein the filters are coated through screen printing or off-set printing.

31. (Previously Cancelled)

32. (Currently Amended) The method of claim 29, wherein the passivation layer is formed of a photosensitive transparent organic material having ~~a~~ good planarization ~~property~~ properties.

33. (Previously Amended) The method of claim 32, wherein the color filters, and the passivation layer are patterned through only exposure and development to form the first contact hole.

34. (Previously Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on an ohmic contact layer;

forming color filters, said filters formed of a photosensitive material and covering the data wire;

forming a passivation layer covering the filters, and formed of a photosensitive transparent organic material having good planarization properties;

forming a first contact hole extending to the drain electrode via the passivation layer and color filters; and

forming a pixel electrode connected to the drain electrode through the first contact hole, wherein

the color filters, and the passivation layer are patterned through only exposure and development to form the first contact hole,

the gate wire further includes a gate pad that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and the color filter, the passivation layer, and the gate insulating layer have a second contact hole and a third contact hole respectively exposing the gate pad and the data pad, and

further comprising a step of forming a redundant gate pad and a redundant data pad that are formed of the same layer as the pixel electrode and respectively connected to the gate pad and the data pad through the second contact hole and the third contact hole.

35. (Previously Amended) The method of claim 29, wherein the gate wire or the data wire is formed of a photosensitive conductive material.

36. (Original) The method of claim 35, wherein the gate wire and the data wire are patterned through only exposure and development.

37. Cancelled

38. (Previously Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on an ohmic contact layer;

forming color filters, said filters formed of a photosensitive material and covering the data wire and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters,

wherein the source electrode and the drain electrode are separated by a photolithography process using a data wire pattern, and the data wire pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

39. (Original) The method of claim 38, wherein a mask used for forming the data wire pattern has a first, a second, and a third part, a transmittance of the third part is higher than the first part and the second part, a transmittance of the first part is higher than the second part, the data wire pattern includes positive photoresist material and the mask is aligned such that the first, the second, and the third parts respectively face the first, the second, and the third portions of the data wire pattern in an exposing step.

40. (Original) The method of claim 39, wherein the first part of the mask includes a partially transparent layer.

41. (Original) The method of claim 39, wherein the first part of the mask includes a pattern smaller than the resolution of the exposure used in the exposing step.

42. (Original) The method of claim 39, further comprising a step of forming an ohmic contact layer pattern between the data wire and the semiconductor.

43. (Original) The method of claim 42, wherein the data wire, the ohmic contact layer pattern, and the semiconductor pattern are formed in the same photolithography process.

44. (Previously Amended) The method of claim 43, wherein steps of forming the semiconductor pattern, the ohmic contact layer pattern, and the data wire comprise:

depositing a semiconductor layer, an ohmic contact layer, and a data conductor layer on the gate insulating layer;

exposing the data conductor layer through a mask;

forming the data wire pattern such that the second portion lies on the data wire by developing of the data conductor layer;

forming the data wire, the ohmic contact layer pattern, and the semiconductor pattern respectively formed of a the data conductor layer, the ohmic contact layer, and the semiconductor layer by removing a portion of the ohmic contact layer under the third portion and

the underlying semiconductor layer, the first portion and the ohmic contact layer under the first portion, and a partial thickness of the second portion.

45. (Previously Amended) The method of claim ~~44~~, wherein the step of forming the data wire, the ohmic contact layer pattern, and the semiconductor pattern comprises:

removing the portion of the ohmic contact layer under the third portion and the semiconductor layer by dry etching along the first portion to expose the gate insulating layer and to complete the semiconductor pattern formed of the semiconductor layer, and

removing the data conductor layer under the first portion and the underlying ohmic contact layer to complete the data wire and the ohmic contact layer pattern.

46. (Currently Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a gate wire formed on an insulating ~~film~~ substrate and comprising:

a gate line; and

a gate electrode connected to the gate line;

a gate insulating layer covering the gate electrode;

a semiconductor pattern formed on the gate insulating layer;

a data wire including a source electrode and a drain electrode, and a data line connected to the source electrode;

a passivation layer covering the data wire and having a first contact hole exposing the drain electrode;

color filters formed under the passivation layer; and

a pixel electrode connected to the drain electrode through the first contact hole,

wherein the gate wire or the data wire are formed of a ~~photodefinable~~ photosensitive conductive material.

47. (Previously Cancelled)

48. (Previously Amended) The thin film transistor array panel of claim 46, wherein the passivation layer and the color filters are formed of a photosensitive material.

49. (Currently Amended) The thin film transistor array panel of claim 46, wherein the photosensitive conductive material is formed of Ag paste or a copper organic metal including photoresist.

50. (Previously Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode;

forming color filters, said color filters covering the data wire and formed of a photosensitive material including resins;

forming a light blocking layer formed of the photosensitive material and covering the semiconductor pattern between the source electrode and the drain electrode when forming the color filters;

forming a contact hole exposing the drain electrode in the color filters; and

forming a pixel electrode connected to the drain electrode through the contact hole.

51. (Previously Amended) The method of claim 50, wherein the color filters are coated through screen printing or off-set printing, or formed through exposure and development process.

52. (Previously Amended) The method of claim 50, further comprising a step of forming a passivation layer covering the color filters after forming the color filters.

53. (Previously Amended) The method of claim 52, wherein the passivation layer is formed of a transparent organic material having good planarization properties.

54. (Previously Amended) The method of claim 50, further comprising a step of forming a buffer insulating layer before forming the color filters.

55. (Previously Amended) The method of claim 50, wherein the light blocking layer is formed of a photosensitive material of red or green resins.

56. (Previously Amended) The method of claim 50, wherein the gate wire or the data wire is formed of a photosensitive conductive material.

57. (Original) The method of claim 56, wherein the gate wire and the data wire are patterned through only exposure and development.

58. (Original) The method of claim 50, wherein the source electrode and the drain electrode are separated by a photolithography process using a data wire pattern, and the data wire pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

59. (Previously Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a gate wire including a gate line and a gate electrode connected to the gate line, and formed on an insulating substrate;

a gate insulating layer covering the gate wire;

a semiconductor pattern formed on the gate insulating layer;

a data wire including a source electrode and a drain electrode, and a data line connected to the source electrode and defining a pixel along with the gate line;

color filters formed of a photosensitive material including resins and respectively formed in the pixel;

a light blocking layer formed on the channel portion of the semiconductor pattern between the source electrode and the drain electrode and formed of the photosensitive material; and

a pixel electrode connected to the drain electrode through a contact hole of the color filter.

60. (Previously Amended) The thin film transistor array panel of claim 59, further comprising a passivation layer that covers the color filters, and the light blocking layer, and is planarized.

61. (Previously Amended) The thin film transistor array panel of claim 60, wherein the passivation layer is formed of an acrylic organic material.

62. (Original) The thin film transistor array panel of claim 59, wherein the data wire has the same shape as the semiconductor pattern except for a channel portion.

63. (Previously Amended) The method of claim 59, wherein the light blocking layer is formed of a photosensitive material of red or green resins.

64. (Currently Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a plurality of gate lines formed on an insulating substrate;

a gate insulating layer covering the gate lines;

a plurality of data lines intersecting the gate lines;

an amorphous silicon layer formed under the entire data lines;

an ohmic contact layer interposed between the data lines and the amorphous silicon layer;

an array of thin film transistors, each transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode;

a plurality of color filters formed over the gate insulating layer, the color filters at least partially overlapping the data lines ~~at last in part~~; and

a plurality of pixel electrodes formed on the color filters, each pixel electrode electrically connected to the drain electrode.

65. (Previously Amended) The thin film transistor array panel of claim 64, wherein each of the pixel electrodes overlaps at least one of the data lines a least in part.

66. (Previously Cancelled)

67. (Previously Amended) The thin film transistor array panel of claim 64, further comprising a storage electrode formed of the same layer as the gate lines.

68. (Previously Amended) The thin film transistor array panel of claim 67, further comprising a conductor pattern overlapping the storage electrode, the conductor pattern formed of the same layer as the data lines.

69. (Original) The thin film transistor array panel of claim 64, wherein adjacent two of the color filters overlap each other at least in part.

70. (Original) The thin film transistor array panel of claim 64, further comprising an insulating layer interposed between the color filters and the pixel electrodes.

71-80. (Previously Cancelled)